Using a Negative Capacitance to Increase the Tuning Range of a Varactor Diode in MMIC Technology

Svilen Kolev, *Member, IEEE*, Bruno Delacressonnière, *Member, IEEE*, and Jean-Luc Gautier, *Senior Member, IEEE*

***Abstract*—An original method to increase the tuning range of a monolithic-microwave integrated-circuit (MMIC) varactor diode is presented in this paper. An active circuit simulating a negative capacitance is connected to the varactor diode. This method allows to increase the varactor's tuning range more than ten times and to compensate its series resistance at the same time. A MMIC simulating a negative capacitance have been successfully fabricated and measured. To the best of the authors' knowledge, this is the first realization of a MMIC simulating a negative capacitance.**

***Index Terms*—Immitance converters, MMICs, MODFETs, varactors.**

I. Introduction

THE main difficulties in the design of tunable active circuits in monolithic-microwave integrated-circuit (MMIC) high electron-mobility transistor (HEMT) technology are due to the insufficient performance of the tunable elements. Tunable active filters and voltage-controlled oscillators (VCOs) most often employ varactor diodes in their structures. In the case of wide-band VCOs, the frequency range covered $f_{\max}/f_{\min}$ is proportional to the square root of the varactor's tuning range $C_{\max}/C_{\min}$. In addition, the VCO phase noise strongly depends on the quality factor of the tunable element.

However, in HEMT processes, the varactor diodes are somewhat degenerated since they are obtained on the basis of HEMTs, and the capacitance effect is mainly caused by modulation of the two-dimensional electronic gas (2DEG). The typical tuning range $C_{\max}/C_{\min}$ of a MMIC varactor is about 2–3 units, if the device's series resistance is to be kept reasonable. Typical series resistance of a MMIC varactor varies from several ohms to several tens of ohms. In addition, this resistance depends on the device's bias voltage [1].

This paper describes a method to increase the tuning range of varactor diodes in HEMT technology and, at the same time, to compensate their series resistance by connecting in series or in parallel an active circuit simulating a negative capacitance.

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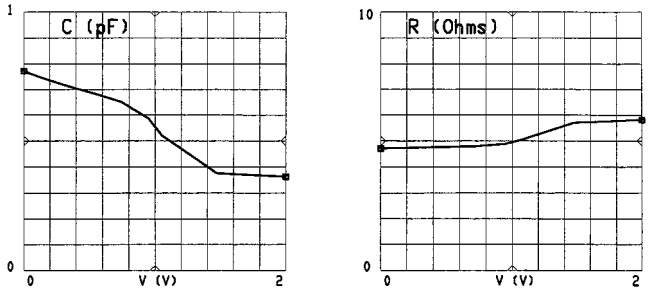

Fig. 1. Tuning characteristics of a DIGM-type 6 × 100 μm Philips varactor in the ED02AH pHEMT process.

II. Characteristics of Varactor Diodes in HEMT Technology

Fig. 1 presents the performance of a MMIC varactor diode in the 0.2-μm-gatelength pseudomorphic high electron-mobility transistor (pHEMT) process ED02AH of Philips-PML, Limeil, France [1]. This device has a total electrode width of 6 × 100 μm.

The tuning range $C_{\max}/C_{\min}$ of this device is 2.1 units and its series resistance is about 5 Ω for a reverse-bias voltage ranging from 0 to 2 V. There is another type of varactor diodes in the ED02AH process, i.e., the bottom electrode interdigited diode (DIBE)-type, with an electrode length of 3 μm instead of 0.2 μm. It allows to obtain tuning ranges of about 12 units, but the series resistance is very bias dependent and can attain several tens of ohms, depending on the device's width. If one wishes to limit this resistance, the tuning range is reduced to about 1.5 units, depending on the total width of the device. These tuning range and series resistance values are typical for all MMIC HEMT processes.

III. Circuit Design and Characterization

A. Principle of Operation

The series association of a negative capacitance (an element whose admittance can be written as $Y = -j\omega C$) and a tunable positive capacitance with a tuning range from $C_{\min}$ to $C_{\max}$ is represented in Fig. 2.

Assuming that these two elements are lossless, the resulting capacitance is

$$C_{eq} = \frac{CC_n}{C + C_n}. \tag{1}$$

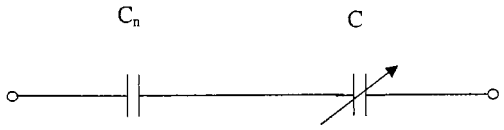

Fig. 2. Series association of a negative capacitance C_n and a tunable positive capacitance C.

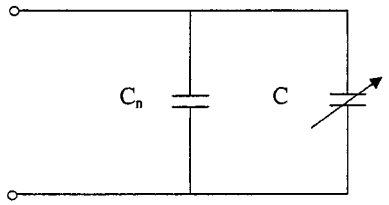

Fig. 3. Parallel association of a negative capacitance C_n and a tunable positive capacitance C.

In order to obtain a positive capacitance, we must take $|C_n| > C_{\max}$. Let us pose $C_n = -kC_{\max}$, where $k > 1$. According to (1), we then have

$$C_{eq\,\max} = \frac{-C_{\max}kC_{\max}}{C_{\max} - kC_{\max}} = \frac{k}{k-1}C_{\max}$$

and

$$C_{eq\,\min} = \frac{-C_{\min}kC_{\max}}{C_{\min} - kC_{\max}}. \tag{2}$$

If $D = C_{\max}/C_{\min}$ is the tuning dynamics of the tunable positive capacitance C, the tuning dynamics D′ of the series association can be written as

$$D' = \frac{C_{éq\,\max}}{C_{éq\,\min}} = \frac{k}{k-1}\left(D - \frac{1}{k}\right). \tag{3}$$

When the coefficient k is close to 1, e.g., $|C_n|$ is close to $C_{\max}$, it can be clearly seen that the tuning dynamics of the series association can reach very high values.

The parallel association of a negative capacitance and a tunable positive capacitance with a tuning range from $C_{\min}$ to $C_{\max}$ is represented in Fig. 3.

Assuming that these two elements are lossless, the resulting capacitance is

$$C_{éq} = C + C_n. \tag{4}$$

In order to obtain a positive capacitance, we must take $|C_n| < C_{\min}$. Let us pose $C_n = -kC_{\min}$, where $k < 1$. According to (4), we then have

$$\begin{aligned} C_{eq\,\max} &= C_{\max} + C_n \\ C_{eq\,\min} &= C_{\min} + C_n. \end{aligned} \tag{5}$$

$D = C_{\max}/C_{\min}$ being the tuning dynamics of the tunable positive capacitance C, the tuning dynamics of the parallel association can be written as

$$D' = \frac{C_{éq\,\max}}{C_{éq\,\min}} = \frac{C_{\max} + C_n}{C_{\min} + C_n} = \frac{D-k}{1-k}. \tag{6}$$

When the coefficient k is close to 1, e.g., $|C_n|$ is close to $C_{\min}$, it is seen that the tuning dynamics of the parallel association can reach very high values.

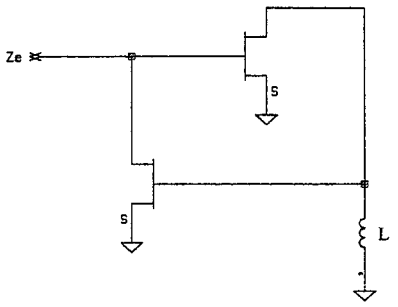

Fig. 4. Principle schematic of the NIC-based negative capacitance.

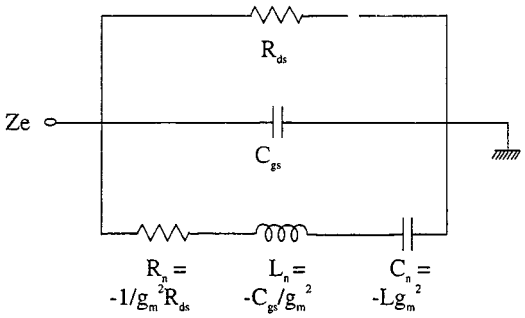

Fig. 5. Equivalent circuit of the negative capacitance.

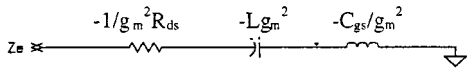

Fig. 6. Simplified equivalent circuit.

In this section, we have shown that the series (and parallel) association between a tunable positive capacitance and a negative capacitance allows to obtain an equivalent capacitance with a significantly increased tuning dynamics.

B. Negative Capacitance

This circuit is based on a negative-impedance converter, designed with two common-source transistors and loaded with an inductor (Fig. 4) [1], [2].

The two common-source stages are forming a negative-impedance converter, which is loaded with the inductive load L. The equivalent circuit, obtained using a three-element HEMT model ($C_{\rm gs}$, g_m, $R_{\rm ds}$) and supposing that the two transistors are identical, is shown in Fig. 5.

If the operating frequency is much smaller than the characteristic frequency

$$f_1 = \frac{g_m^2 R_{\rm ds}}{2\pi C_{\rm gs}} = f_t g_m R_{\rm ds} \approx 16 f_t \tag{7}$$

where f_t is the cutoff frequency of the transistors, the influence of the parallel elements is negligible and the equivalent circuit can be reduced to that of Fig. 6.

Let us also notice that, for a field-effect transistor, the product $g_m R_{\rm ds}$ is much greater than 1 and independent of the gatewidth. It is equal to about 16 for a Philips pHEMT of the ED02AH process.

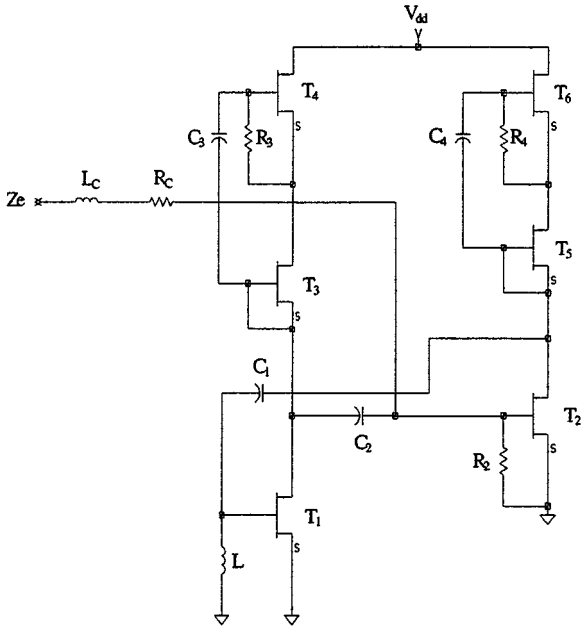

Fig. 7. Schematic diagram of the negative capacitance.

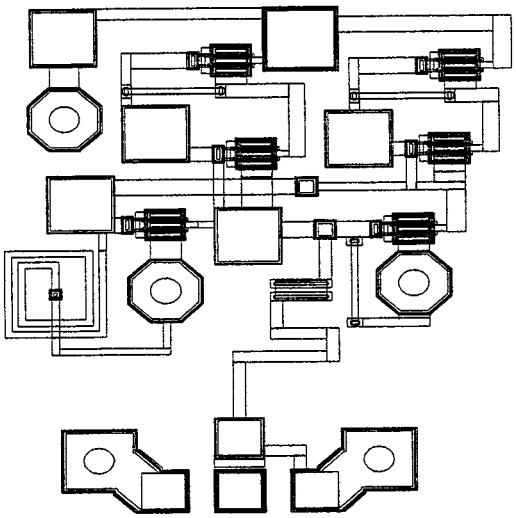

Fig. 8. Layout of the negative capacitance.

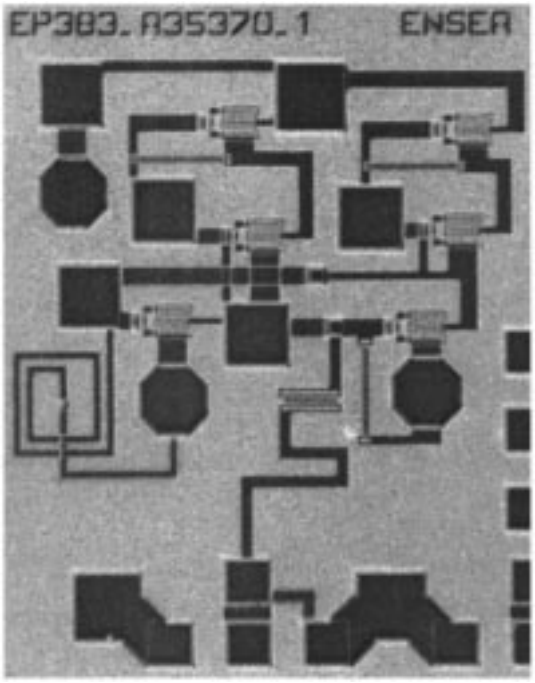

Fig. 9. MMIC negative capacitance.

This is a series *RLC* circuit. The negative resistance and the negative inductance can be compensated by placing a resistor and an inductor of proper values at the circuit's input. Thus, we obtain a negative capacitance equal to $-Lg_m^2$, where L is the value of the load inductor and g_m^2 is the transconductance of the pHEMTs.

C. Simulation and Measurement Results of the Negative Capacitance

The complete schematic of the negative capacitance is shown in Fig. 7.

In order to demonstrate the feasibility of a MMIC simulating a negative capacitance, a circuit has been designed and fabricated using the 0.25-μm-gatelength pHEMT process H40 of GEC-Marconi, Caswell, U.K. The circuit's layout is shown in Fig. 8.

The pHEMTs are two-gate finger devices with a total gatewidth of 2×60 μm. They are biased using cascode active loads because of the high load that they represent. The inductor L is the load of the negative impedance converter. In [1], we show that its resistive loss introduces a negative resistance in parallel with the negative capacitance in the equivalent circuit of Fig. 5, thus reducing the bandwidth of the compensation of the negative resistance $-1/g_m^2 R_{\rm ds}$ in the equivalent circuit. The value of the inductor and its series resistive loss have been optimized for a good compensation over a large bandwidth [1].

At the input of the circuit, we have also placed two compensation elements—an inductor, actually realized with transmission lines, and a resistor, which compensate the circuit's intrinsic negative inductance and negative resistance, respectively (Fig. 6). In the circuit's layout, we have also placed a parallel capacitor of about 2.6 pF at the input (not shown in the schematic diagram of Fig. 7) in order to obtain a total positive capacitance (a negative capacitance alone cannot be measured because it oscillates). This parallel capacitor is integrated only to be able to measure the circuit; in a real application, it would not be needed (the negative capacitance will be connected to another sub-circuit, e.g., a varactor diode). We should, however, notice that this capacitor and the transmission lines connecting it to ground resonate at about 12 GHz (in our case), thus limiting the circuit's bandwidth. On the same chip, we have realized separately the same positive capacitor of 2.6 pF in order to be able to measure it precisely and to extract the negative capacitance. We have also realized on the same chip several test structures, i.e., a transistor and an inductor, to be able to estimate the technological variations of the process.

Fig. 9 presents a photograph of the MMIC negative capacitance.

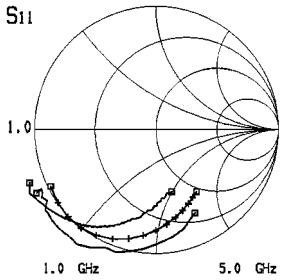

Fig. 10. Post-layout simulation and measurement results of the circuit including the parallel positive capacitor at the input.

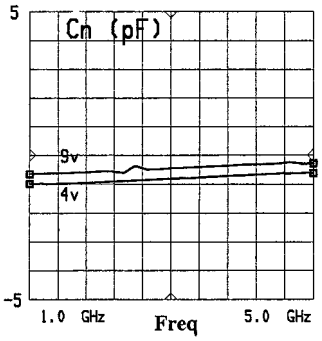

Fig. 11. Extracted negative capacitance at $V_{\rm DD} = 4$ V and 9 V.

The circuit's active surface is 0.8 × 0.8 mm^2. Post-layout simulation and measurement results of the complete circuit are shown in Fig. 10.

The crossed-line trace in the middle shows the post layout simulated S_{11} of the circuit. The inner and outer traces represent the measured S_{11} at $V_{\rm DD} = 4$ V and 9 V, respectively. The negative resistance observed is due to the technological variations of the transconductance g_m of the transistors. Remember that the circuit's intrinsic negative resistance (Fig. 5) is equal to $-1/g_m^2 R_{\rm ds}$. The test transistors manufactured separately on the same chip showed variations of g_m as high as 20%, which are typical to the H40 process [1]. Using a more precise process would allow to obtain a virtually pure negative capacitance in a much larger bandwidth (0.2–12 GHz) [1]. The extracted negative capacitance is shown in Fig. 11.

We obtain a negative capacitance of about -1 pF at $V_{\rm DD} = 4$ V. The compensation of the intrinsic negative inductance (equal to $-C_{\rm gs}/g_m^2$) turns out to be incomplete because its value has been modified by the technological variations of g_m and $C_{\rm gs}$ during processing.

D. Series Association of a Negative Capacitance and a Varactor Diode

Fig. 12 shows the schematic of the circuit. The varactor diode D is biased via two high-value resistors, i.e., R_1 and R_2.

All pHEMTs are 2 × 50 μm devices. The negative capacitance is equal to -0.8 pF. The circuit's intrinsic negative resistance R_n (see the equivalent circuit of Fig. 5) is about $-10\ \Omega$. The compensation resistor R_c is chosen 5.8 Ω and the compensation inductor L_c (realized with a transmission line) is equal to 0.16 nH. Thus, we obtain a series *RC* circuit with $C = -0.8$ pF

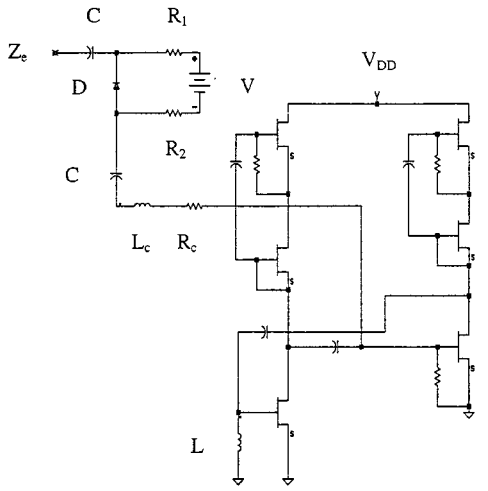

Fig. 12. Series association of a negative capacitance and a varactor diode.

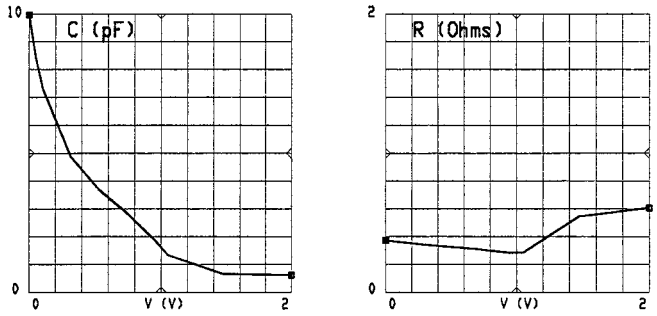

Fig. 13. Series association: simulation results at 2 GHz with the complete foundry models of all elements.

and $R = -4.2\ \Omega$. The negative resistance that results compensates the series resistance of the varactor diode. It can also be shown [1] that the resonant frequency of the series association is reduced $\sqrt{k/(k-1)}$ times approximately compared to the resonant frequency of the varactor diode alone. The resonant frequency of the series association in this case is 7.5 GHz.

The simulation results (HP-MDS) with the complete foundry models of all elements, taking into account their parasitics, are shown in Fig. 13.

The capacitance is varying from 10 to 0.62 pF for a reverse-bias voltage of the varactor diode ranging from 0 to 2 V. Thus, the tuning range $C_{\rm max}/C_{\rm min}$ of this series association is 16 units and its serial resistance is about 0.4 Ω. We have been able to increase about eight times the tuning range of the varactor diode and to compensate its serial resistance at the same time.

E. Parallel Association of a Negative Capacitance and a Tunable Positive Capacitance

The advantage of the parallel association is that the bandwidth of the resultant capacitance is not reduced by the multiplication factor k, unlike the series association. Unfortunately, the parallel association of a negative capacitance and a varactor diode does not allow to obtain better results compared to the series association [1] because of the high series resistance and low tuning dynamics of the varactor diodes at our disposal. In [1], we have

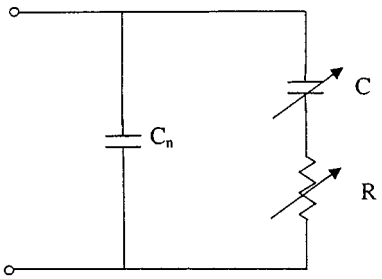

Fig. 14. Parallel association of a negative capacitance and a nonideal tunable capacitance.

proven that when $|C_n|$ is close to $C_{\min}$, the equivalent series resistance of the resultant capacitance can reach several $k\Omega$, which would make such a capacitance virtually useless.

When the tunable capacitance is lossy (Fig. 14), the impedance of the parallel association is given by

$$\begin{aligned} Ze &= \frac{\frac{1}{j\omega C_n}\left(R+\frac{1}{j\omega C}\right)}{R+\frac{1}{j\omega}\left(\frac{1}{C}+\frac{1}{C_n}\right)} \\ &= \frac{R}{\left(1+\frac{C_n}{C}\right)^2+\omega^2 C_n^2 R^2} \\ &\quad + \frac{-j\omega C_n R^2+\left(1+\frac{C_n}{C}\right)\frac{1}{j\omega C}}{\left(1+\frac{C_n}{C}\right)^2+\omega^2 C_n^2 R^2}. \end{aligned} \tag{8}$$

The real part of Ze increases when $|C_n|$ approaches C. At low frequencies, the association's maximum resistance is given by

$$R'_{\max} = Re(Ze)_{\max} \approx \frac{R}{\left(1+\frac{C_n}{C_{\min}}\right)^2} = \frac{R}{(1-k)^2}. \tag{9}$$

If $R = 5\,\Omega$ and we wish to impose $R'_{\max} = 20\,\Omega$, we obtain $k = 0.5$. According to (6), we have

$$D' = \frac{C_{éq\,\max}}{C_{éq\,\min}} = \frac{D-k}{1-k} = 2D-1. \tag{10}$$

Thus, the tuning range of the nonideal parallel association is limited by the maximum series resistance that we impose. In this case ($k = 1$), the new tuning range D' is less than two times greater than the original tuning range D.

We have replaced the varactor diode with a specially designed active circuit [1], i.e., a "capacitance multiplier" (not shown here), whose input capacitance can be tuned by varying its bias voltage. The post-layout simulation results (Fig. 15) confirm the high value of the series resistance of the association when $|C_n|$ approaches C. For example, at 2 GHz, we obtain a tunable capacitance from 0.44 to 8.8 pF. The series resistance reaches its maximum (33 Ω) when $C = 0.44$ pF.

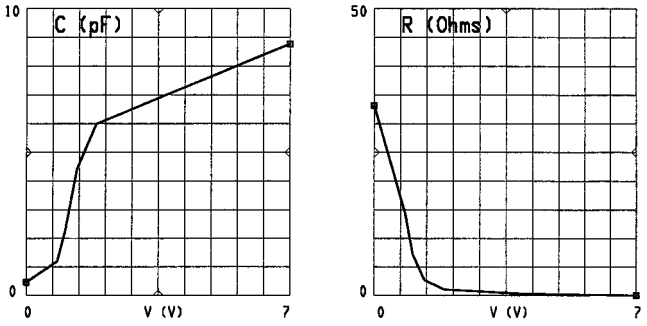

Fig. 15. Parallel association of a negative capacitance and a nonideal tunable capacitance (a capacitance multiplier here): post layout simulation results at 2 GHz.

IV. Conclusion

An original method to increase the tuning range of MMIC varactor diodes has been presented in this paper. A negative capacitance has been associated in series to the varactor diode. The feasibility of a negative capacitance in MMIC technology has been demonstrated. To the best of our knowledge, this has been the first time that the feasibility of "active" varactors has been investigated.

Acknowledgment

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